REMARKS/ARGUMENTS

In the Office Action mailed May 29, 2009, claims 1-14 were rejected. In response, Applicants hereby request reconsideration of the application in view of the below-provided remarks. No claims are amended, added, or canceled.

Claim Rejections under 35 U.S.C. 101

Claims 1-14 were rejected under 35 U.S.C. 101 as purportedly lacking patentable utility. In particular, the Office Action contends that the claimed invention is directed towards controlling program logic on a microcontroller, specifically, executing programmatic behavior steps. The Office Action also asserts that once the execution of the programmatic behavior step occurs, no tangible output is produced. The Office Action further submits transitioning thru programmatic behavior steps without producing a tangible result lacks utility.

However, Applicants respectfully submit that there is no basis for the stated rejection. There is no requirement that the claimed invention must produce some kind of tangible output. Section 101 states:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Furthermore, the MPEP states:

> If at any time during the examination, it becomes readily apparent that the claimed invention has a well-established utility, do not impose a rejection based on lack of utility. An invention has a well-established utility if (i) a person of ordinary skill in the art would immediately appreciate why the invention is useful based on the characteristics of the invention (e.g., properties or applications of a product or process), and (ii) the utility is specific, substantial, and credible.

Applicants assert that the claimed invention qualifies under both requirements i) and ii) of the MPEP. Additionally, per the language of Section 101, Applicants assert that the claimed invention is directed towards patentable utility. Specifically, Applicants direct attention to the Specification of the instant application; therein can be found several examples of the utility of embodiments of the claimed invention. One example of the utility of an embodiment of the claimed invention is described in page 3, lines 3-14 of the specification. This portion describes utility of an embodiment of the claimed invention in increasing the difficulty in making conclusions regarding the process or data in the current action of a microcontroller from the perspective of an outside observer or attacker. Thus, for example, the security of a system may be increased by an embodiment of the claimed invention.

Therefore, Applicants respectfully submit claims 1-14 satisfy the requirements set forth in the MPEP with respect to determining whether a claimed invention complies with 35 U.S.C. 101. Accordingly, Applicants request that the rejection of claims 1-14 under 35 U.S.C. 101 be withdrawn.

Claim Rejections under 35 U.S.C. 112, first paragraph

Claims 12 and 13 were rejected under 35 U.S.C. 112, first paragraph, as purportedly failing to comply with the written description requirement. Specifically, the Office Action states that the limitation "wherein the one of the different instruction sequences is located at the program address" of claims 12 and 13 lacks support within the original disclosure.

Applicants submit that the remarks in the current Office Action do not fully consider the response submitted by Applicants. In particular, Applicants provided two individual citations to point out and describe support for the claimed language of "program address" within the specification. For at least this reason, Applicants respectfully request reconsideration of the response below in its entirety.

In the previous response, Applicants respectfully submitted that the limitation related to one of the different instruction sequences located at the program address is supported by the specification, even though there may not be explicit antecedent basis for the language. This language is supported by the specification, for example, at least on

page 3, lines 3-14, which states "the desired action can be selected from a large number of possible instruction sequences by the use of a Random Number Generator" (emphasis added) and "By means of a random program run of this kind." While the above section of page 3, lines 3-14, does not explicitly refer to the different instruction sequences located at the program address, the description at page 1, lines 14-29, describes how different instructions are associated with memory locations or program addresses.

In response to the current rejection, Applicants maintain the previous response and even though the reasoning in the Office Action, mailed 01/04/2010, reasserts that the "cited specification does not mention the limitation element 'program address' " (page 12, Response to Arguments), Applicants again assert that the description at page 1, lines 14-29, explicitly describes the use of program addresses or values. The cited language is clear and descriptive, and it appears that the response included in the Office Action is based solely on the first above-cited portion of the specification. However, both of the cited portions support the indicated claim language. Therefore, Applicants respectfully submit that the detailed description of the specification provides support for each of these claim limitations because embodiments of the process are described to realize jumps or branches based on conditions to determine how the instructions at each location or program address proceed.

While the specification may not explicitly provide antecedent basis for the exact language used in the claims, Applicants respectfully submit that the indicated language finds considerable support in the specification, including the support described above. See, MPEP 608.01(o) ("an applicant is not limited to the nomenclature used in the application as filed"). Furthermore, 37 C.F.R. 1.75(d)(1) requires the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable. In other words, support is required, and antecedent basis is simply one way of providing support, but is not the only way to provide support for the limitations of the claim.

Here, although the language of the claims differs somewhat from the actual nomenclature provided in the specification, Applicants respectfully submit that the claim language is nevertheless supported by the specification because the claims recite limitations that are well within the scope of the embodiments described in the

specification. Moreover, although the MPEP indicates that the use of a variety of terms can be confusing, Applicants respectfully submit that the terms used in the claims do not cause such confusion. On the contrary, the language of the claims is ascertainable from the specification, as shown by the explanation provided above.

Therefore, Applicants assert the claims are supported by the specification as filed because the language is within the scope of the written description provided in the specification, and the language does not cause confusion as to the meaning of the claims. Accordingly, Applicants respectfully request that the rejections of claims 12 and 13 under 35 U.S.C. 112, first paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. 103

Claims 1-14 were rejected based on one or more cited references. The cited reference(s) relied on in these rejections include:

Cohen (EP 0690370 A2, hereinafter Cohen)
Anderson et al. (U.S. Pat. Pub. No. 2003/0084336, hereinafter Anderson)

In particular, claims 1-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen in view of Anderson. However, Applicants respectfully submit that these claims are patentable over Cohen and Anderson for the reasons provided below.

Independent Claim 1

Claim 1 is patentable over the combination of Cohen and Anderson because the rejection of claim 1 is improper. The rejection of claim 1 is improper because 1) the Office Action does not establish a *prima facie* rejection for claim 1, and 2) the proposed combination of Cohen and Anderson is improper because the proposed combination would render Cohen unsatisfactory for its intended purpose.

Applicants respectfully reaffirm Applicants' assertions made in response to the previous Office Action, mailed 5/29/2009, and re-state the arguments with further elaboration, explanation, and evidence to support the specific reasoning. In particular,

Applicants assert that the reasoning presented below shows that there is substantial evidence against the suggested combination of references asserted by the Office Action. For example, Applicants submit that the suggested combination is improper because the combination suffers from a lack of rational underpinning and is improper. Specifically, the proposed combination is improper because the articulated reasoning is not supported by the references. Also, the device of Cohen to provide an alert to an outside system, provide selective timing compatibility, and generate state signals for the process of the microcontroller would be insufficient for at least these intended purposes.

Lack of *Prima Facie* Rejection

In order to establish a *prima facie* rejection of a claim under 35 U.S.C. 103, the Office Action must present a clear articulation of the reason why the claimed invention would have been obvious. MPEP 2142 (citing *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398 (2007)). The analysis must be made explicit. Id. Additionally, rejections based on obviousness cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. Id.

Here, the Office Action fails to provide an explicit reason as to why the limitations of claim 1 would have been obvious. In particular, the Office Action simply states:

> Cohen does not expressly teach the use of a Random Number Generator (RNG) for purposes of microcontroller activity (e.g., controlling a Jump Condition).
>
> However, the feature using a random number generator to control microcontroller activity was ready available and was well known in the art at the time of applicant's original filings and would have been an obvious modification of the system disclosed by Cohen as introduced by Anderson. Anderson discloses the use of a RNG for control of microcontroller activity (e.g., controlling a Jump Condition with in the microcontroller) (to provide microcontroller architecture such that the internal activities of the microcontroller are controlled by a RNG [par. 23]):
>
> Therefore, given Anderson's ability to control microcontroller activity using programmatic behavior steps, a person having ordinary skill in the art at the time of the invention would have recognized the

desirability and advantage of modifying Cohen to enhance the security and speed of performing the steps thereby enhancing the microcontroller's activity by employing the well known feature of a microcontroller utilizing random number generation means to control its activity disclosed above by Anderson.

Office Action, 01/04/2010, page 5.

The Office Action is merely conclusory in stating that the proposed modification of Cohen would "enhance the security and speed of performing the steps." Applicants submit that the Office Action offers no explicit analysis to support the assertion that the proposed modification would afford such an improvement. Additionally, there is no analysis as to how the proposed modifications would be implemented into the system of Cohen because the system of Cohen teaches a security aspect which reacts upon detection or tampering. Cohen, page 7, line 27, to page 8, line 45. Therefore, it is not obvious how the proposed modification would "enhance the security" of the system. Additionally, there is no analysis to show how the proposed modification might enhance the speed of the system taught by Cohen because there does not appear to be an advantage in the proposed combination over the system of Cohen relating to processing speed or reduction in the number of processes. Therefore, Applicants submit that there is no showing or explanation of how it would be obvious to combine the cited references, or that the indicated limitation might otherwise be obvious in light of the cited references. Moreover, in addition to the lack of showing and analysis in support of the proposed combination, Applicants submit that there is substantial evidence against the suggested combinations for reasons further described below.

Therefore, the Office Action fails to establish a *prima facie* rejection for claim 1 because the Office Action does not provide articulated reasoning with some rational underpinning in the rejection of claim 1. Accordingly, Applicants respectfully submit that the rejection of claim 1 under 35 U.S.C. 103(a) should be withdrawn because the Office Action fails to establish a *prima facie* rejection.

The Proposed Combination is Improper

Furthermore, even if the combination of Cohen and Anderson were to teach all of the limitations of the claim, the proposed combination of Cohen and Anderson is

nevertheless improper. In asserting a combination of references as a basis for an obviousness rejection, the proposed combination or modification cannot change the principle of operation of the prior art. MPEP 2143.01(VI). In addition, the combination of references cannot render the prior art unsatisfactory for its intended purpose. MPEP 2143.01(V). Here, the combination of teachings proposed in the Office Action would change the principle of operation of Cohen and would render the device of Cohen unsatisfactory for its intended purpose.

The proposed combination of Cohen and Anderson is improper because the use of a random number generator, as taught by Anderson, within the device of Cohen would render the device of Cohen unsatisfactory for its intended purpose. Anderson generates pseudo-random bits with a free-running pseudo-random number generator based on a shift register. The bit stream generated by the pseudo-random number generator is sampled upon execution of a set-random-carry command. Anderson, paragraph 23. In contrast, Cohen teaches that the performance of a conditional robust jump is dependent upon the contents and integrity of the composite condition signal within a single machine cycle. Cohen, page 8, line 43 to page 9, line 4; Fig. 7. In other words, the jump is decided based on conditions within the microcontroller. The jump is determined by the integrity of the data which allows a GoError signal to be activated.

Nevertheless, despite the teaching of Cohen that the jump is dependent on the data integrity, the Office Action proposes to modify the teaching of Cohen to use a random number generator bit stream to trigger the jump, instead of a data integrity check. This proposition to use a random number generator not only removes the use of the code taught by Cohen (Cohen, page 9, lines 10-25) to perform a jump based on data integrity, but further would appear to eliminate the ability for the teachings of Cohen to generate the GoError signal because this modification would, in turn, prevent the system from informing the outside world of a data integrity problem, as taught by Cohen. Moreover, the teachings of Cohen are directed towards a tamper-resistant system which employs the use of a security comparator and a security sensor array to detect an "expected state" within the device of Cohen. Cohen, page 7, lines 23-51. These components execute various lines of code taught by Cohen in order to adapt to and prevent compromise due to tampering. This is different from the system of Anderson which employs a random

number generator. If the proposed modification of Cohen were implemented as suggested by the Office Action the combination would render the entire security and signal sensitive "conditional jump" of Cohen unsatisfactory for its intended purpose. Nevertheless, without support or offering of evidence, the Office Action asserts:

> "...it would have been obvious to those skilled in the art to perform the modification in order to enhance the performance and security of Cohen's microcontroller activity."
> Office Action (01/04/2010, page 12, Response to Arguments, 103 Remarks)

Applicants assert that the reasoning provided in the Office Action does not find support in the teachings of either Cohen or Anderson because there is no support for the assertions of "enhanced performance and security."

Furthermore, the Office Action does not address or recognize the timing sensitive aspect of the device of Cohen. Specifically, Cohen teaches a balance of speed and optimization which allows the processor to be selectibly timing compatible with an existing processor. Cohen, page 2, lines 23-30. It appears that the random nature of the proposed combination would not facilitate this aspect of the invention and would further render the device of Cohen unsatisfactory for its intended purpose.

Moreover, even if it were possible to implement the teaching of Anderson without replacing the aforementioned teachings of Cohen, the proposed modification of Cohen would also make it difficult or impossible to prevent conflicting signals from occurring with respect to controlling and tracking the jump signals because the jump criteria for Cohen and Anderson are dissimilar. Furthermore, there is no explanation of how the random number generator approach of Anderson might be implemented into the teachings of Cohen without rendering Cohen unsatisfactory for, first, communicating an error signal upon detection of a data integrity compromise and preventing a jump or branch in the microcontroller and, second, associating the jump with a signal received from an instruction decoder because Anderson teaches use of a random number generator to control jumps and branches in the program of the microcontroller.

Therefore, combining the references of Cohen and Anderson, as proposed in the Office Action, would render the device of Cohen unsatisfactory for its intended purpose

because use of the bit sampling of the bit stream generated by the random number generator described in Anderson would prevent the system of Cohen from performing a jump based on data integrity, from demonstrating selectable timing compatibility with an existing processor, and, further, would appear to prevent Cohen from generating the GoError signal which would further prevent the device of Cohen from informing the outside world of a data integrity problem. Accordingly, Applicants respectfully assert independent claim 1 is patentable over the cited references because the proposed combination of references is improper.

Independent Claims 5 and 11

Applicants respectfully assert independent claims 5 and 11 are patentable over the proposed combinations of Cohen and Anderson at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Each of claims 5 and 11 recites subject matter which is similar to the subject matter of claim 1 discussed above. Although the language of these claims differs from the language of claim 1, and the scope of these claims should be interpreted independently of other claims, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of these claims.

Dependent Claims

Claims 2-4, 6-10, and 12-14 depend from and incorporate all of the limitations of the corresponding independent claims 1, 5, and 11. Applicants respectfully assert claims 2-4, 6-10, and 12-14 are allowable based on allowable base claims. Additionally, each of claims 2-4, 6-10, and 12-14 may be allowable for further reasons.

CONCLUSION

Applicants respectfully requests reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/mark a. wilson/

Date: March 31, 2010

Mark A. Wilson
Reg. No. 43,994

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111